A 17-bit Oversampling ADC for RFID Tags

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ABSTRACT

This paper presents a fourth-order tri-level quantizer based delta-sigma modulator. The modulator adopts topology of cascade of integrator with multiple feedback for higher stability even swing insides the loop filter is higher. Which demands high power operational amplifier. The modulator signal transfer function STF shows a low-pass response. While the noise transfer function NTF shows the high pass response, to shapes the quantization noise at higher frequencies. To improve the modulator's performance, the NTF zero optimization method is applied.. The modulator signal-to-noise ratio (SNR) without NTF zero optimization technique is 90 dB while with NTF zero optimization technique SNR is 104 dB. The out-of-band gain (OBG) of adjusted to 1.5 for higher stability of the fourth-order loop filter. The zeroes of the NTF which are poles of the loop filter needs to at DC of unit circle. The zero optimization techniques shift the zeroes of the NTF to further remove the quantization noise from the signal band. Limited DC gain, limited slew-rate, and gain-bandwidth product were researched because integrators want optimal operational amplifiers.. The modulator model also investigated for circuit non-idealities thermal noise, flicker noise to get an estimate for the performance degradation. The fourth-order tri-level modulator with an oversampling ration (OSR) of 64 can achieve SNR of 106 dB as with full-scale input of 550 mV.

Keywords: Out-of-band Gain, Noise transfer function, Signal transfer function, DC gain, Operational amplifier

1. INTRODUCTION

A fourth-order tri-level delta-sigma modulator is modeled and simulated for RFID Tags. The modulator can achieve 17-bit resolution with an oversampling ratio of 64. The complete modulator modeled for circuit non-idealities like limited DC gain, thermal noise, and limited Slew-rate. A 450 MHz incident RF signal provides power and a reference clock for this 1 mm/sup 2/ wireless telemetry device, which transmits data as a binary phase shift keyed signal on a 900 MHz carrier. The gadget generates a 3 V/sub DC supply from the -12.3 db incident RF wave. In the United States, this equates to a working distance of more than 18 metres. A 3-bit ID tag plus the output of an on-chip 5-bit single-slope analog-to-digital converter make up the transmit data (ADC). While operating, the entire IC drains 4 mWA 12bits SAR ADC is presented, along with preliminary results, for autonomous multi-sensor systems. The comparator and DAC have been designed to consume the least amount of power possible. With a 1.2-V supply, the proposed device consumes 0.52µW at a bit-clock of 50 kHz and 0.85µW at a bit-clock of 100 kHz. As far as we know, the 66 fJ/conversion-step Figure-of-Merit is the best reported thus far. A 0.35 mm2 NXP CMOS 0.14m chip was used to construct the ADC. Only four metal layers were used to ease the sensors' 3D integration. For autonomous multi-sensor systems, an ultra-low power 12bit (SAR) ADC with innovative design and measurement results is presented. The comparator and DAC have been

engineered to use as little power as possible. The suggested device consumes 0.52W at a bit-clock of 50 kHz and 0.85W at a bit-clock of 100 kHz with a 1.2-V supply. The Figure-of-Merit for this implementation is 66 fJ/conversion-step. With a 0.35 mm2 area, the ADC was manufactured utilizing NXP CMOS 0.14m technology. Only four metal layers were used to enable for 3D sensor integration. In general, the design of a sensor interface for passive RFID tags is investigated. The ISO/IEC 15693 and ISO/IEC 14443 standards impose power and temporal constraints on HF RFID tags, which are explored in this fashion. There is a survey analysis of the best analog-to-digital converters for inactive Radio Frequency identification detecting, as well as a general multi-sensor interface proposed. It is suggested that you use the appropriate converter type and architecture. Finally, a carbon nanotube gas sensor interface is proposed, along with a brief overview of the circuits used and preliminary results. We split the most significant bit and least significant bit determination processes with the two independent ADC circuits of the Incremental Sigma Delta ADC in order to improve conversion speed. While the 1st Incremental Delta Sigma ADC is operating on the other input, the 2nd Incremental Delta Sigma ADC conversion begins. When compared to a normal Extended Counting Incremental Sigma Delta ADC, the Analog to Digital conversion speed is improved by two times by determining the MSB and LSB individually. When processing the input of the 2nd Incremental Sigma Delta ADC, which is the output of the switched capacitor integrator within the 1st Incremental Sigma Delta ADC block, the inverting sample/hold circuit inverts it. Because the digital circuit size is larger than the analogue circuit area, the increased active area is relatively tiny as a result of the extra analogue circuit. In this study, a 14 bit Extended Counting Incremental Sigma-Delta ADC with a single 2.5 V supply voltage is created in 0.25 m CMOS technology. The conversion speed is roughly 150k samples/sec at a clock rate of 25 MHz.. The 1 MSB has a voltage of 0.02 V. 0.50 x 0.35 mm2 is the active area. 1.7 mW is the average power consumption [5].

This work presented a delta-sigma modulator with a fourth-order tri-level quantizer. Even if the swing inside the loop-filter is larger, the modulator employs a cascade of integrators with multiple FF design for improved stability. This necessitates a high-power operational amplifier. The modulator's signal transfer function responds with a low-pass response. The noise transfer function (NTF) illustrates the high pass response, which forms the quantization noise at higher frequencies. The modulator's performance is improved using the NTF zero optimization technique. The modulator signal-to-noise ratio (SNR) is 90 dB without NTF zero optimization, but 104 dB with NTF zero optimization. The fourth-order loop filter's out-of-band gain (OBG) was increased to 1.5 for improved stability. The loop filter's poles, which are NTF zeroes, must be at the DC of the unit circle. The NTF's zeroes are shifted using zero optimization techniques to further reduce quantization noise from the signal band. Limited DC gain, limited slew-rate, and gain-bandwidth product were researched because integrators want optimal operational amplifiers. To predict the performance degradation, the modulator model looked into circuit non-idealities such as thermal noise and flicker noise. With an oversampling ration (OSR) of 64, a fourth-order tri-level modulator

may produce an SNR of 106 dB with a full-scale input of 550 mV.

Following the introduction, the second section discusses the design of the modulator with CIFB topology, while the third section describes the modelling and simulation of the modulator as well as the operational amplifier for integrator for the implementation of the fourth-order tri-level modulator design. Finally, part four brings the paper to a close.

2. MODULATOR DESIGN

A higher order with four integrators in the loopfilter and tri-level quantizer modulator modeled using Delta-Sigma Toolbox. The cascade of integrators with multiple feedback (CIFB) investigate for higher out-of-band-gain (OBG) of 1.5 with moderate oversampling ratio of 64 without NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 108 dB with OSR of 64. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The coefficients of the proposed fourth order multiple bit CIFB obtained from Delta-Sigma Toolbox [12]. These coefficients represent the ratio of capacitors at the discrete-time implementation of the modulator. Then these coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency. Those coefficients which are not mentioned, have value zero. the modulator NTF and STF is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 1.5. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The figure 2 shows transient output of the modulator. While Figure-3 displays the zeroes and poles of loop-filter as well as NTF in more details. It is shown that NTF zeroes On the DC, lies in the unit circle. While the Figure 4 shows for the suggested modulator's STF and NTF plot. The output power spectral density plot with SNR of 108, achieving effective number of bit

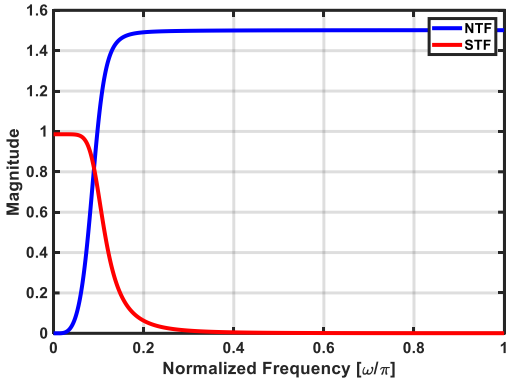

Figure 1: STF and NTF plot (CIFB)

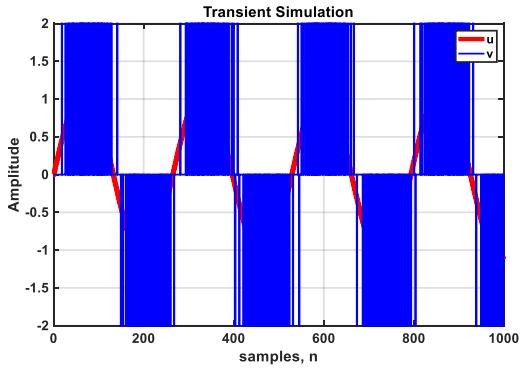

Figure 2: STF and NTF plot (CIFB)

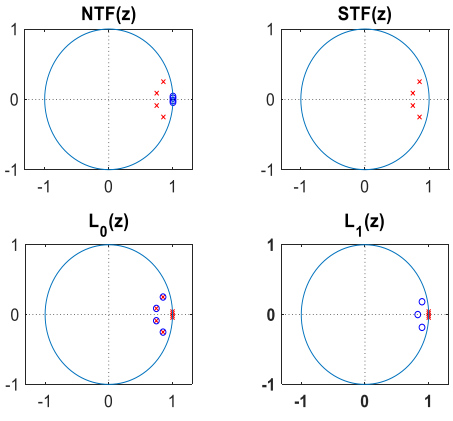

Figure 3: Unit circle plot (CIFB)

(ENOB) of 17-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loop-filter is assumed having infinite DC gain. The noise floor is at the level of -120dB, the quantization noise is suppressed maximum with four integrators inside the loop filter. Due to moderate OSR of 64, the signal bandwidth is small. Due to CIFB topology of the modulator the signal swing inside the loop-filter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loop-filter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loop-filter.

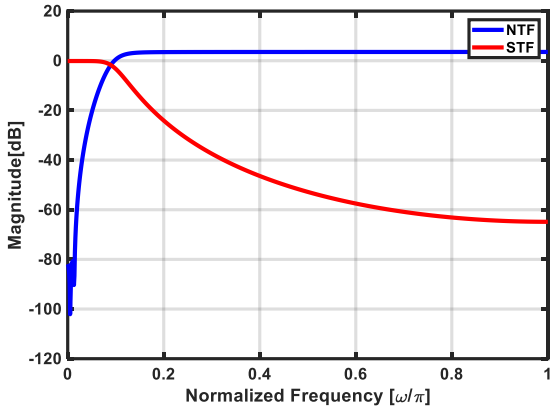

Figure 4: STF and NTF plot (CIFB)

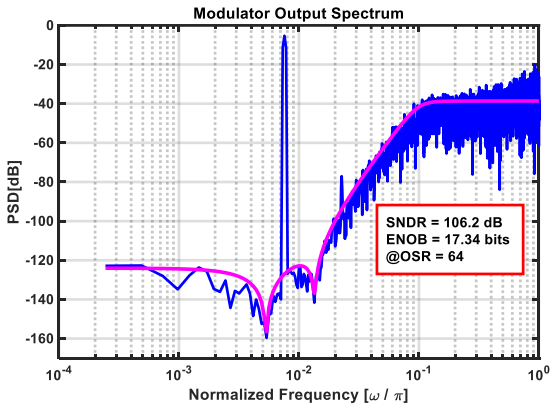

Figure 5: Output PSD plot (CIFB)

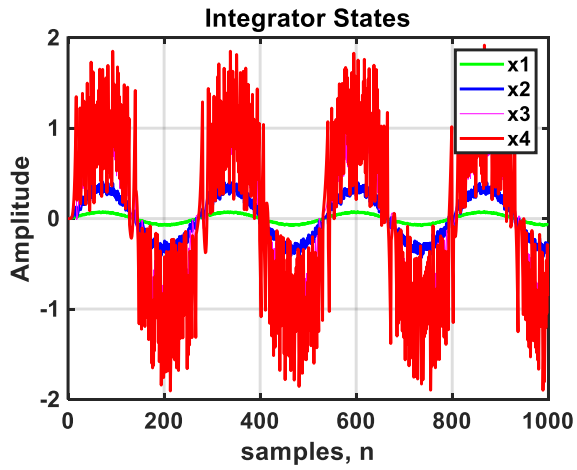

Figure 6: Output states of the integrators

3. RESULTS & DICUSSION

A fourth-order tri-level modulator for RFID tags is proposed. The topology of the modulator is CIFB for higher stability. The modulator can achieve SNR of 106 dB with OSR of 64 with OBG of 1.5. The simulation environment SDToolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

The modulator was modelled as a fourth-order tri-level delta-sigma modulator, and simulations revealed that it can attain an SNR of 106 dB. To gain an assessment of the modulator's SNR performance, the circuit non-idealities are modelled and simulated. To improve the modulator's performance, the Noise transfer function zero optimization technique is applied. Without NTF zero optimization technique, the modulator signal-to-noise ratio (SNR) is 90 dB, however with the NTF zero optimization

method, the SNR is 104 dB. For better fourth-order loop filter stability, the out-of-band gain (OBG) was increased to 1.5. The loop filter's poles, which are NTF zeroes, must be at unit circle's DC. The NTF's zeroes are shifted using zero optimization techniques to decrease quantization noise from the signal band even more. Because integrators require ideal operational amplifiers, limited DC gain, partial slew-rate, and gain-bandwidth product were studied. The fourth-order tri-level modulator with an oversampling ration (OSR) of 64 can achieve SNR of 106 dB as with full-scale input of 550 mV.

5. ACKNOWLEDGMENT

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